WHAT IS CLAIMED IS:

1. A system comprising:

N different memories wherein N> 1;

M different busses with each one of the busses having a bandwidth to transport data at a predetermined rate, operatively coupled to one of the N memories wherein M is greater than 1;

a plurality of memory controllers with each one of the plurality of memory controllers operatively coupled to one of the N memories, wherein said each one of the plurality of memory controllers setting an associated memory in a first mode or a second mode; and

an arbiter responsive to at least one memory request signal to generate an Access vector that causes information to be read simultaneously from multiple ones of the N memory set in the first mode wherein total bandwidth on the busses of the multiple ones of the N memories is greater than the bandwidth on a single bus of one of the N memories.

2. The system of Claim 1 wherein the first mode includes a Read mode.

3. The system of claims 1 or 2 wherein each of the N memories includes DDR DRAM.

4. The system of claim 3 wherein each of the DDR DRAM are partitioned into at least four banks and at least one buffer spread across the at least four banks.

5. The system of claim 4 wherein each buffer is partitioned into multiple maskable units.

6. The system of claim 4 wherein each buffer is partitioned into four units.

7. The system of claim 6 wherein each unit is equivalent to 1/4 the size of the buffer.

8. The system of claim 6 wherein each unit is maskable.

9. The system of claim 1 wherein the arbiter includes a controller executing a slice selection algorithm comprising the steps of:

- Exclude slices scheduled for re-fresh cycle (indicated by each DRAM controller)
- Assign slices for all R requests of Transmitter controller
- Complement R-accesses from corresponding EPC queue [Slice; QW]
- Assign slice to EPC for globally W excluded slices (e.g. slice is excluded by all slice exclusion rules from Receiver)
- Assign slices to W requests in RR (Round Robin) fashion between non-excluded slices staring from last assigned slice (slice assigned to Receiver Controller in previous window)
- Complement W-accesses by EPC accesses from corresponding EPC queue [Slice; QW] and
- Assign slice to EPC requests according to priority expressed by Weight.

10. A system including:

a Network Processor including at least one Data Flow Chip, at least one Embedded Processor Complex EPC chip, at least one Scheduler chip wherein the at least one EPC chip and the at least one Scheduler chip are operatively coupled to the at least one Data Flow Chip;

a plurality of memory elements with each one coupled by a separate bus to the at least one Data Flow Chip;

a first high speed data port that transmits data out of the Data Flow Chip; and

an arbiter operatively coupled to the Data Flow Chip, said arbiter being responsive to Read (R) Requests to cause multiple ones of the bus to transmit data from associated memory elements simultaneously wherein the combined data bandwidth on the multiple ones of the bus is sufficient to meet Bandwidth requirements of the high speed port.

11. The system of claim 10 wherein the bandwidth on each bus includes approximately 7.75 Gbps.

12. The system of claim 10 or claim 11 wherein the bandwidth of the high speed port includes approximately 10 Gbps.

13. The system of claim 10 further including a second high speed data port that transmits data into the Data Flow Chip.

14. The system of claim 10 or claim 13 further including a Receiver Controller operatively coupled to the second high speed data port, said Receiver Controller generating and providing Write (W) request signals to the arbiter;

EPC Interface Controller, operatively coupled to the EPC chip, generating and providing Read(R)/Write(W) Request signals to the arbiter; and

a transmitter controller, operatively coupled to the scheduler chip and the first high speed port, generating and providing the Read(R) Requests to said arbiter.

15. The system of claim 14 wherein the arbiter prioritizes the requests.

16. The system of claim 14 wherein priority 1, the highest, is assigned to the transmitter controller, priority 2, the second highest, is assigned to the Receive Controller and priority 3, the lowest, is assigned to the EPC controller.

17. The system of claim 14 wherein the arbiter includes circuit arrangement that allows access of the Receive Controller or the EPC Controller to memories not selected by the transmitter controller.

18. The system of claim 10 wherein the memory elements include N DDR DRAMs, N >1.

19. The system of claim 18 wherein each one of the N DDR DRAMs includes multiple banks.

20. The system of claim 19 wherein the each one of the N DDR DRAMs is partitioned into at least one buffer spreading across the multiple banks.

21. The system of claim 20 wherein the at least one buffer is further partitioned into smaller buffers.

22. The system of claim 21 wherein the at least one buffer is approximately 64 bytes and each one of the smaller buffers is approximately 16 bytes.

23. A method comprising the acts of:

providing a plurality of separate memory elements in which frames from communication device is to be stored or retrieved;

partitioning the frame with a controller into at least two parts;

storing each one of the at least two parts into different memory elements if the at least two parts are adjoining parts of the same frame.

24. The method of claim 23 further including the acts of an arbiter in response to a request causing the memories to be read simultaneously wherein each one of the two parts is

available simultaneously on respective busses associated with each one of the memory elements.

25. A method including the acts of:

providing a plurality of separate memories in which data is stored;

receiving in an arbiter a request to read data from selected ones of said plurality of separate memories; and

simultaneously reading said memories to provide data simultaneously on individual busses coupled to the selected ones of said plurality of separate memories.

26. The method of claim 25 wherein the bandwidth of data on each individual bus is less than the total bandwidth on activated busses.

27. A method comprising the acts of:

providing a plurality of separate memory modules in which frames from communication devices can be stored;

partitioning a frame into multiple parts;

writing adjacent parts of the frame in different ones of the memory modules; and

simultaneously accessing multiple memory modules in a single memory access window to read data therefrom wherein the total bandwidth of data output from the multiple memory modules matches the bandwidth of a FAT pipe port on a communication device.

28. The system of claim 9 wherein the controller includes a state machine or other hardware circuits.